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Design and Development of a Single Channel Analyzer with Microcontroller Based Controlled Output

M. N. Islam[1], H. Akhter[2], M. Begum[3], K. Asaduzzaman[4], M. S. Alam[5], M. A. S. Haque[6] and M. Hoq[7]

[1,2,3] Electronics Division, Atomic Energy Centre, Bangladesh Atomic Energy Commission, P.O. Box No. 164, Dhaka, Bangladesh.
[4,5,6,7] Institute of Electronics, Atomic Energy Research Establishment, Bangladesh Atomic Energy Commission, G.P.O Box 3787, Savar, Dhaka, Bangladesh.

Abstract— *Single Channel Analyzer (SCA) is a most common device used in today's nuclear world. Therefore, A SCA with microcontroller based controlled output has been proposed in this article. The system comprises of Lower Level Discriminator (LLD), Upper Level Discriminator (ULD), wide dynamic range, Fast Processing and Hysteresis. The Comparator LM339N used as the key component that performs the main function of the proposed nuclear module. The multi-turn potentiometers have been used as LLD and ULD for the incoming linear pulses from shaping amplifier. The system has also employ the Hysteresis facilities so that oscillations due to stray feedback are not possible. A lower pin and less housing PIC microcontroller (P16F676) has been used to control the width and time delay of the output pulses.*

Keywords—Integral Discriminator, Differential Discriminator, Comparator, PIC Microcontroller and MPLAB IDE.

I. INTRODUCTION

Single Channel Analyzer is a linear-to-logic converter in widespread use involves two independent discrimination levels.

This discriminator produces a logic output pulse if the input pulse amplitude lies between two levels. The action of the unit is therefore to select a band of amplitudes or window in which the input amplitude must fall in order to produce an output pulse [1]. In this regard, a fast zero dead-time single channel analyzer for nuclear spectroscopy applications describes a new approach of designing SCA with an emphasis on accelerator-based X-ray absorption fine structure (XAFS) has been presented [2]. Design and construction of an accurate timing single channel analyzer (TSCA) for the timing of pulses over a wide dynamic range gives an overview of the timing methods and uncertainty factors as "walk and jitter"[3]. In the present research, two mode single channel analyzer with microcontroller based controlled width and timing of the output pulses ,fast processing and few front panel control have been presented.

II. METHODOLOGY

2.1: Block Diagram

Fig.1 shows the block diagram of the complete system below comprises of comparator circuit (integral and differential application) and microcontroller (P16F676) circuit for timing delay.

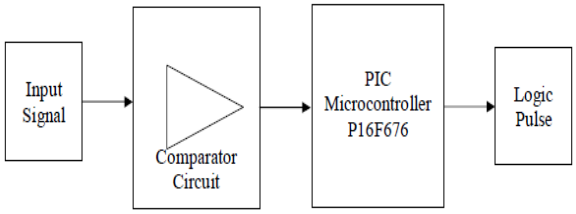

Fig.1: Shows the block diagram of the complete system.

2.2: Schematic Diagram

The Schematic Diagram of the Complete System has been shown in fig.2.

2.2.1. Input Circuit: The SCA input has resistor R_1 tied to common of non-inverting pin in IC2A, IC2B and IC2C.

2.2.2. Lower Level Discriminator1: The Lower Level Discriminator1 (LLD1) consists of Potentiometer (Pot1) maintains 0-5 V.

2.2.3. Lower Level Discriminator2: The Lower Level Discriminator1 (LLD2) has a Potentiometer (Pot2) maintains 0-5 V.

2.2.4. Upper Level Discriminator: The Upper Level Discriminator (ULD) comprises of Potentiometer (Pot3) varies from 0-10 V.

2.2.5. Lower Level Hysteresis Ckt.1: The Lower Level Hysteresis Ckt.1 consists of Input Resistor, R_1 and

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Variable Resistor (VR_1) which gives the hysteresis as VR_1/R_1.

2.2.5. Lower Level Hysteresis Ckt.2: The Lower Level Hysteresis Ckt.2 has Input Resistor, R_1 and Variable Resistor (VR_2) which gives the gain as VR_2/R_1.

2.2.6. Upper Level Hysteresis Ckt.:The Upper Level Hysteresis Ckt. consists of Input Resistor ,R_1 and Variable Resistor (VR_3) which gives the gain as VR_3/R_1.

2.2.7. First Comparator Ckt.: The first comparator circuit has one of four precision voltage comparators IC2A to eliminate the system noise operation of the single channel analyzer in integral mode.

2.2.8. Second Comparator Ckt.: The second comparator circuit has another precision voltage comparator IC2B to set the system LLD operation of the single channel analyzer in differential mode.

2.2.9. Third Comparator Ckt.: The third comparator circuit has third precision voltage comparator IC2C to set the system ULD operation of the single channel analyzer in differential mode.

2.2.10. True Comparator Ckt.: The true comparator circuit has rest of the four precision voltage comparators IC2D to prohibit the falls operation of the single channel analyzer in differential mode.

2.2.11. Microcontroller Circuit: The microcontroller circuit is the heart of the developed system comprises of Flash-Based 8-Bit CMOS Microcontroller PIC 16F676 14 pin DIP Package. The device consists of Built-in-Oscillator, CPU, 2-ports: PortA and PortC, Reset, Memory for data and Program, Interrupts and free-run timer TMR0 and so on [4]. An assembly language program has been developed by using MPlab Integrated Development Environment (IDE) to control the timing of the logic outputs both positive and negative.

2.2.12. Integral Mode Enable Ckt: The integral mode enble circuit has been designed with mode selection switch (MS1) and a series resistor, R_2 for diminishing bouncing effect.

2.2.13. Integral Mode Interrupt Ckt.: The differential mode interrupt circuit receives interrupt input in RA2 of IC5 (P16F676).

2.2.14. Integral Mode Outputs: The differential mode positive and negative outputs are available at RA0 and RA1 of IC5 (P16F676) through R_5 and R_7 respectively.

2.2.15. Differential Mode Enable Ckt: The differential mode enble circuit has been constructed with mode selection switch (MS2) and a series resistor, R_6 for diminishing bouncing effect.

2.2.16. Differential Mode Interrupt Ckt.: The differential mode interrupt circuit receives interrupt input in RA2 of IC1 (P16F676).

2.2.17. Differential Mode Outputs: The differential mode positive and negative outputs are available at RA0 and RA1 of IC1 (P16F676) through R_4 and R_3 respectively.

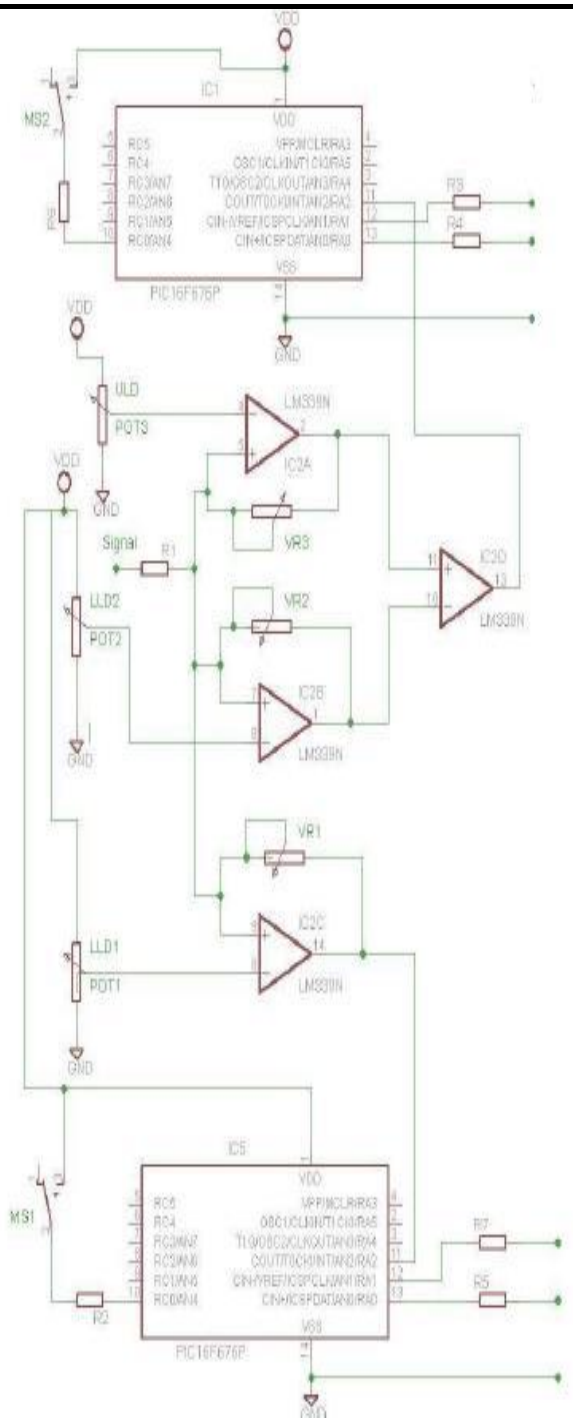

Fig.2: Shows the schematic diagram of the complete system.

2.3: Circuit Operation

The fig.3 and fig.4 describe the operating principle of the constructed nuclear module. When the leading edge of the incoming linear pulse just crosses the discrimination level then the module generate an output logic pulse. The fig.5 shows the program flow chart for the proposed system. The fig.6 shows the input and output wave form of the SCA.

In the present system, the lower-level discriminator (LLD) and upper-level discriminator (ULD) are independently adjustable from front panel controls. The

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module has two modes of operation like integral discriminator and the differential discriminator or SCA. These two modes can be controlled by two simple on-ff switches. An assembly language program for less pin configuration microcontroller PIC16F676 has been developed by using MPlab Integrated Development Environment (IDE) to control the timing of the logic outputs both positive and negative.

The integral discriminator is for just to eliminate system noise so that all those events in the detector that deposit full energy of an incident radiation can be measured. The differential discriminator or window is set to correspond only to those events in the detector that deposit full energy of an incident radiation. In this way, one type or energy of radiation often can be measured selectively in the presence of other radiations. Thereafter, nuclear counting system is being used to count the radioactive particles coming from a source or nuclear installations for environmental monitoring and detecting health hazards. These pulses can be also applicable for DAC and MCA.

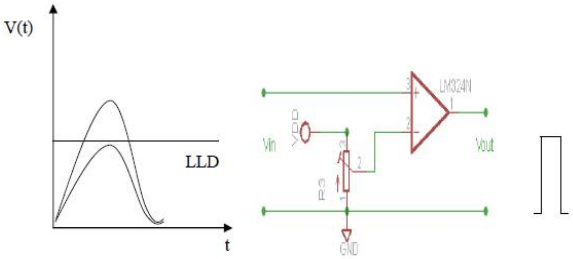

Fig.3: Shows the operating principle of the SCA: integral mode

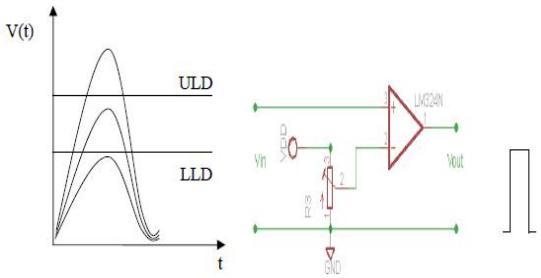

Fig.4: Shows the operating principle of the SCA: differential mode

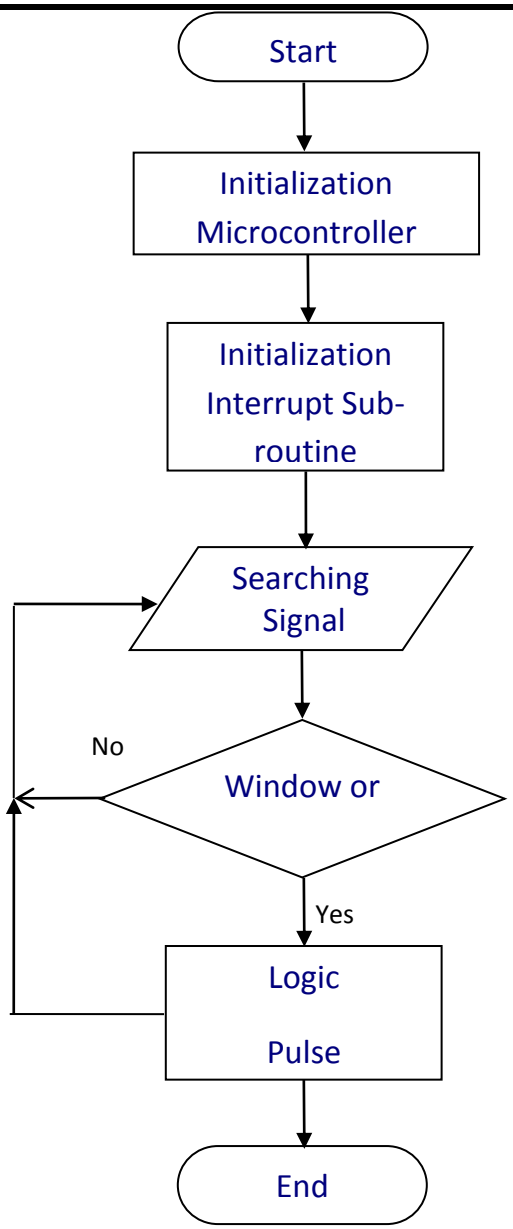

Fig.5: Shows the program flow chart of the proposed system.

2.4: Results and Discussion

In this module, the lower level discriminator (LLD) 1 & 2 can be varied independently from 0-5V from front panel control. The upper level discriminator (UDL) also can be varied from 0-10V. The module has positive feedback (hysteresis) facilities. The system comprises of program level delay and pulse width controller by using microcontroller (P16F676) starting from 1µs. The fig.5 shows the program flow chart for the proposed system.

It has been observed from 20-channel integral discriminator that output pulse amplitudes for all the channels approach to supply voltage. While the supply voltage was 5.0V, the output logic pulse amplitude for the same has been observed as 4.36V to 4.72V. The discriminator outputs have large pulse width as seen from

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9.66 µs to 18.07 µs as shown in fig.6. There were no positive or negative overshoot. At the end, Threshold or noise level can be selected from some µV to supply as the board has been designed with multi-turn potentiometers. In the present case, the threshold levels were from 50.71 mV to 57.64 mV [5,6].

The selected LM339 consists of four independent precision voltage comparators, with an offset voltage specification as low as 20mV max for each comparator, which were designed specifically to operate from a single supply over a wide range of voltages [7].

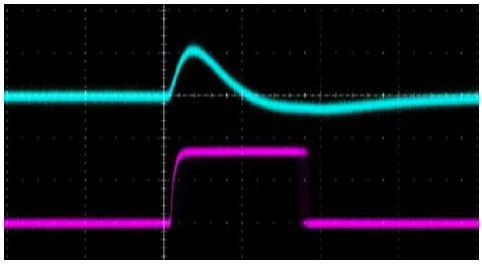

Fig.6: Shows the input and output wave form of the SCA.

III. CONCLUSION

A single channel analyzer (SCA) with microcontroller based controlled output has been presented in this research. The fig.3 and fig.4 describe the operating principle of the designed nuclear module. And the fig.6 shows the input and output wave form of the SCA. The system comprises of two distinct modes of operation and incurred with both positive and negative outputs. The system has LLD, ULD, wide dynamic range, Fast Processing and Hysteresis. The system is simple, reliable, efficient in operation and user friendly. The module can be used for in any nuclear measurement chain, nuclear counting system, DAC and MCA applications successfully.

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